REMARKS

In the Drawings

The Examiner states that Figure 5 should be designated by a legend such as –Prior Art— and requests that a Replacement Drawing in compliance with 37 CFR 1.121(d), be submitted. The Examiner cited Paragraph [0039] of the Present Application in the objection, which refers to the "older systems such as the system 500 of figure 5." Applicant respectfully traverses this objection and believes that the system 500 shown in Figure 5 is not prior art for the following reasons.

Applicant notes that Paragraphs [0036]-[0039] of the Present Application state, in part:

[0036] With initialization starting with the availability of Vcc, a Flash memory device of the present invention does not require the hardware signal RP# for operation and to begin initialization. Therefore, a Flash memory device of the present invention can operate with host controllers that do not have a way for providing a hardware initialization signal to the Flash memory, such as RP#.

[0037] However, a Flash memory device of the present invention does require a software "STOP" signal to stop the initialization cycle. . . . This requires in some cases the appropriate software routines to be loaded into the system and/or host controller. Loading theses software routines can be problematic if there is no other source of storage for the routines than the Flash memory of the present invention. . . . Therefore a secondary source of non-volatile storage that does not require such initialization must exist in systems where in the host controller requires loading of software routines to issue the "STOP" command and allow access of the Flash memory of the present invention.

[0038] One such a system is shown in Figure 5, wherein a processor/host controller 502 is coupled to an SDRAM memory device 504 and a synchronous Flash memory device 506. A non-volatile memory device 508 containing BIOS code is also coupled to the processor/host controller 502. In the system of Figure 5, the non-volatile memory device 508 containing the BIOS code of the system 500, also contains the software routines necessary for the system to access the synchronous Flash memory device 506 and issue the "STOP" command to end its looping initialization cycle. In Figure 5, as above, the processor/host controller 502 is

defined to include, but is not limited to, an integrated chipset, or a processor, or other system capable of interfacing with embodiments of the present invention.

[0039] The system of Figure 5 is more commonly found in computer systems of older age with a separate slower bus for the BIOS memory. As host controllers that require loading of software routines to issue the "STOP" command also tend to be in older systems, the older systems such as the system 500 of Figure 5 could be easily modified to accommodate the synchronous Flash memory devices of the present invention by simply modifying the BIOS code. Such ability allows for easy retrofit of existing systems to include synchronous Flash memory of the present invention.

Applicant therefore maintains that Paragraph [0039] refers to the architecture of the system (in that it includes a separate asynchronous bus to couple to an asynchronous flash memory BIOS for the system to initially boot from) represented by Figure 5 as being of an older style which has been modified to incorporate and interoperate with an embodiment of the present invention, as clearly stated in Paragraphs [0036]-[0039] of the Present Application. In particular, the Applicant notes that the system 500 of Figure 5 is shown as incorporating a synchronous Flash memory device 506. As such, Applicant maintains that the system shown in Figure 5 is not prior art. Applicant also maintains that the statement cited by the Examiner, "older systems such as the system 500 of figure 5," is not an admission of prior art but simply a reference to this system 500 as being an older system architecture style. Applicant therefore respectfully requests that the Examiner's objection to Figure 5 be withdrawn because the system illustrated in Figure 5 is not old and thus is not prior art.

In the Specification

In the Title

The Examiner states that the title of the invention is not descriptive. Applicant respectfully traverses this objection and notes that the specification, while describing synchronous flash memory does not restrict embodiments of the invention to synchronous flash memory devices. Applicant also notes that the original claims 8-9, 11-14, 16, 22-26 and 37-38 recite generic memory devices or flash memory devices and are thus not restricted to synchronous flash memory devices. Applicant therefore respectfully maintains that the present title "Power-Up Initialization for Memory" is appropriate and requests that the title not be

changed to "Power-Up Initialization for Synchronous Flash Memory," as suggested by the Examiner.

In the Disclosure

The Examiner states that the disclosure is objected to because of the following informalities: In Paragraph [0039], "loading theses" should be –loading these--. Applicant was unable to locate an error in Paragraph [0039] or the term "loading theses." However, Applicant did find the recited typographical error, "loading theses," in Paragraph [0037], and has therefore accordingly amended Paragraph [0037] to correct "Loading theses" to "Loading these." Applicant respectfully submits that the amendment to the specification has been made to fix a typographical error. As such, Applicant contends that no new matter has been added by this correction. Applicant therefore respectfully requests that the Examiner's objection to the description be withdrawn.

Claim Rejections Under 35 U.S.C. § 112

Claim 32 was rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement and the enablement requirement.

Applicant respectfully traverses the rejection. Applicant maintains that claim 32 contains subject matter that was described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

Applicant notes that claim 32 recites that the separate bus is a non-synchronous bus. Applicant respectfully maintains that various forms of memory devices and busses, including synchronous and asynchronous memory devices and busses, are well known in the art and that the Applicant is allowed to rely upon the knowledge of one skilled in the art for written description and enablement. (*See*, MPEP §2163(II)(A)(3)(a), §2163(II)(A)(3)(a), and §2163.02). Applicant also respectfully submits that asynchronous and synchronous memory controllers, asynchronous and synchronous memory buses, and asynchronous and synchronous volatile and non-volatile memory devices are detailed in the Application, at least, by Figures 1, 4, and 5 and by the Specification at Paragraphs [0006]-[0007] and [0038]-[0039]. Figure 5 shows a separate non-volatile memory device 508 containing BIOS code that is coupled to the Processor/Host Controller 502, by a separate slower bus. (*See*, Present Application, Page 9, Paragraphs [0038]-

[0039]). Paragraph [0007] describes SDRAM as differing from conventional DRAM in that it synchronizes itself with the bus. (*See*, Present Application, Page 2, Paragraph [0007]). Applicant therefore maintains that, since asynchronous and synchronous memory devices and busses are defined by the specification and that they are well known by those skilled in the art, that non-synchronous busses (any memory bus that is not synchronous) is therefore described and enabled.

On written description, Applicant notes that MPEP §2163.02 states that the "standard for determining compliance with the written description requirement is, 'does the description clearly allow persons of ordinary skill in the art to recognize that he or she invented what is claimed.' *In re Gosteli*, 872 F.2d 1008, 1012, 10 USPQ2d 1614, 1618 (Fed. Cir. 1989). . . . *Ralston Purina Co. v. Far-Mar-Co., Inc.*, 772 F.2d 1570, 1575, 227 USPQ 177, 179 (Fed. Cir. 1985) (quoting *In re Kaslow*, 707 F.2d 1366, 1375, 217 USPQ 1089, 1096 (Fed. Cir. 1983))." And that '[t]he subject matter of the claim need not be described literally (i.e., using the same terms or *in haec verba* in order for the disclosure to satisfy the description requirement." (*See*, MPEP §2163.02))

Applicant further notes that MPEP §2163.04 states that the burden is on the Examiner with regard to the written description requirement, stating "[t]he examiner has the initial burden of presenting by a preponderance of evidence why a person skilled in the art would not recognize in an applicant's disclosure a description of the invention defined by the claims. *Wertheim*, 541 F.2d at 263, 191 USPQ at 97."

On enablement, the Applicant respectfully submits that it is analysis of the claim rejected against the Application as a whole that determines enablement under 35 U.S.C. § 112, first paragraph. *See,* MPEP §2163(II)(A)(2) and MPEP §2163(II)(A)(3)(a).

Applicant also notes that MPEP §2164.04 states that the burden is on the Examiner with regard to the enablement requirement, stating that "[i]n order to make a rejection, the examiner has the initial burden to establish a reasonable basis to question the enablement provided for the claimed invention. *In re Wright*, 999 F.2d 1557, 1562, 27 USPQ2d 1510, 1513 (Fed. Cir. 1993) (examiner must provide a reasonable explanation as to why the scope of protection provided by a claim is not adequately enabled by the disclosure). A specification disclosure which contains a teaching of the manner and process of making and using an invention in terms which correspond in scope to those used in describing and defining the subject matter sought to be patented must be taken as being in compliance with the enablement requirement of 35 U.S.C. 112, first paragraph, unless there is a reason to doubt the objective truth of the statements contained therein which must be relied on for enabling support."

Furthermore, "[w]hat is conventional or well known to one of ordinary skill in the art need not be disclosed in detail. *See, Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d at 1384, 231 USPQ at 94. If a skilled artisan would have understood the inventor to be in possession of the claimed invention at the time of filing, even if every nuance of the claims is not explicitly described in the specification, then the adequate description requirement is met. *See, e.g., Vas-Cath*, 935 F.2d at 1563, 19 USPQ2d at 1116; *Martin v. Johnson*, 454 F.2d 746, 751, 172 USPQ 391, 395 (CCPA 1972) (stating 'the description need not be *in ipsis verbis* [i.e., 'in the same words'] to be sufficient')." *See,* MPEP §2163(II)(A)(3)(a) and §2163(II)(A)(3)(a).

Applicant contends that relevant features of claim 32 have been described in the specification to allow one skilled in the art to practice the invention. Applicant therefore maintains that claim 32 and the term "non-synchronous bus" are considered to be described and enabled by the specification.

The Applicant therefore requests that the rejection of claim 32 under 35 U.S.C. § 112, first paragraph, be withdrawn in that the specification does clearly describe the invention in a way to enable one skilled in the art to make or use the invention.

Claim Rejections Under 35 U.S.C. § 102

Claims 1, 4-10, 12-14, 17-20, 22-31, and 33-36 were rejected under 35 U.S.C. § 102(b) as being anticipated by Applicant's admitted prior art (the AAPA). Applicant respectfully traverses this rejection and submits that claims 1, 4-10, 12-14, 17-20, 22-31, and 33-36 are allowable for at least the following reasons.

In rejecting claims 1, 4-10, 12-14, 17-20, 22-31, and 33-36, the Examiner stated that "[a] synchronous flash memory interface is disclosed in paragraph 7. The synchronous flash memory device beginning initialization upon receiving a power signal (RP#) on a power bus (signals are inherently delivered on a bus) is disclosed in paragraph 28 and in prior art figure 2." Applicant notes that the U.S. Patent Application cited in Paragraph [0007] (United States Patent Application Serial No. 09/627,682, titled "Synchronous Flash Memory") was filed on July 28, 2000 and, as such, does not qualify as prior art published over one year before the date of filing of the Present Application under 35 U.S.C. § 102(b). Applicant further maintains that Figure 2 and Paragraphs [0007] and [0028] also do not qualify as such as they were filed with the Present

Application. Applicant therefore maintains that the Examiner's rejection of claims 1, 4-10, 12-14, 17-20, 22-31, and 33-36 under 35 U.S.C. § 102(b) is thus improper.

In addition, Applicant respectfully submits that Paragraph [0028] of the Present Application describes that the #RP signal is "reset" or "power down" signal that is "released 202 by a compatible synchronous host controller (not shown) after power up," and is therefore not a power signal on a power bus as maintained by the Examiner. The Applicant also respectfully maintains that the AAPA of Figure 2 and Paragraph [0028] of the Present Application teaches a synchronous Flash memory device which begins an initialization cycle only upon release #RP signal and that the initialization stops automatically after a specified time period. *See, e.g.*, AAPA, Figures 1 and 2, Page 6-7, paragraphs [0028]-[0030]. Applicant therefore respectfully submits that AAPA does not teach or disclose a synchronous Flash memory that begins an initialization cycle upon power up and stops the initialization cycle in response to an external command.

Applicant's claim 1 recites, in part, "wherein the synchronous Flash memory device begins an iterating initialization cycle upon receiving a power signal on a power bus, and stops the iterating initialization cycle upon receiving an external command." As detailed above, Applicant submits that the AAPA fails to teach or disclose such a synchronous Flash memory device that begins an iterating initialization cycle upon receiving a power signal on a power bus, and stops the iterating initialization cycle upon receiving an external command. As such, the AAPA fails to teach or disclose all elements of independent claim 1.

Applicant's claim 8 recites, in part, "wherein the memory device commences a continuously looping initialization cycle upon receiving a power signal, and stops the continuously looping initialization cycle upon receiving an external signal." As detailed above, Applicant submits that the AAPA fails to teach or disclose such a memory device that begins an iterating initialization cycle upon receiving a power signal, and stops the iterating initialization cycle upon receiving an external command. As such, the AAPA fails to teach or disclose all elements of independent claim 8.

Applicant's claim 17 recites "[a] method of initializing a synchronous Flash memory device comprising commencing a continuously looping initialization cycle upon receiving a power signal; and stopping the continuously looping initialization cycle upon receiving an external command." As detailed above, Applicant submits that the AAPA fails to teach or disclose such a method. As such, the AAPA fails to teach or disclose all elements of independent claim 17.

Applicant's claim 22 recites "[a] method of initializing a memory device comprising starting a repeating initialization cycle upon receiving a power signal on a power distribution line; and stopping the repeating initialization cycle upon receiving an external command." As detailed above, Applicant submits that the AAPA fails to teach or disclose such a method. As such, the AAPA fails to teach or disclose all elements of independent claim 22.

Applicant's claim 28 recites, in part, a system having a synchronous Flash memory device "wherein the synchronous Flash memory device begins an iterating initialization cycle upon receiving a power signal on a power bus, and stops the iterating initialization cycle upon receiving an external command." As detailed above, Applicant submits that the AAPA fails to teach or disclose such a system having a synchronous Flash memory device that begins an iterating initialization cycle upon receiving a power signal on a power bus, and stops the iterating initialization cycle upon receiving an external command. As such, the AAPA fails to teach or disclose all elements of independent claim 28.

Applicant respectfully contends that claims 1, 17, 22 and 28 have been shown to be patentably distinct from the cited reference. As claims 4-10, 12-14, 18-20, 23-27, 29-31 and 33-36 depend from and further define claims 1, 17, 22 and 28, respectively, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(b) and allowance of claims 1, 4-10, 12-14, 17-20, 22-31, and 33-36.

Claims 37-38 were rejected under 35 U.S.C. § 102(e) as being anticipated by Kessler (U.S. Patent No. 6,820,196). Applicant respectfully traverses this rejection and reserves the right to swear behind the cited reference. The Applicant submits that claims 37-38 are allowable for at least the following reasons.

Applicant respectfully maintains that Kessler teaches a television set-top-box (STB) that checks the contents of and selectively initializes the data contents of an internal Flash memory device upon power up. Applicant has carefully reviewed the reference and has not found reference in Kessler to the internal device initialization that the Flash memory device must perform before it can make itself available on the data bus for read and write access by the processor, as maintained by the Examiner. Applicant respectfully maintains that the cited Figures 1 and 3 of Kessler refer to the system (the STB) powering up, checking the protected/formatted status of the Flash memory, and initializing the Flash memory data contents

if the device is not formatted. (*See, e.g.*, Kessler, Abstract, Figures 1 and 3, Column 1, lines 48-63, and Column 3, lines 10-29). Applicant therefore respectfully submits that Kessler does not teach or disclose a synchronous Flash memory that begins an initialization cycle upon power up and stops the initialization cycle in response to an external command.

Applicant's claim 37 recites, in part, a computer system that has "a memory device coupled to the host controller, wherein the memory device begins to iterate an initialization cycle in response to Vcc, and stops iterating the initialization cycle in response to the host controller." As detailed above, Applicant submits that Kessler fails to teach or disclose such a memory device that begins an iterating initialization cycle in response to Vcc, and stops iterating the initialization cycle in response to the host controller. As such, Kessler fails to teach or disclose all elements of independent claim 37.

Applicant's claim 38 recites a method of operating a computer system "coupling a host controller to a memory device; detecting Vcc in the memory device; starting an iterating initialization cycle in the memory device; and stopping iteration of the initialization cycle in the memory device in response to a software command from the host controller." As detailed above, Applicant submits that Kessler fails to teach or disclose such a method. As such, Kessler fails to teach or disclose all elements of independent claim 38.

Applicant respectfully contends that claims 37-38 have been shown to be patentably distinct from the cited reference. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(e) and allowance of claims 37-38.

Claim Rejections Under 35 U.S.C. § 103

Claims 2-3, 11, 21, and 15-16 were rejected under 35 U.S.C. § 103(a) as being anticipated over Applicant's admitted prior art (the AAPA) in view of "SGS-THOMSON ST10F166 (the ST10F166 reference). Applicant respectfully traverses this rejection and feels that claims 2-3, 11, 21, and 15-16 are allowable for the following reasons.

Applicant respectfully notes that, as stated above in regards to the rejection of independent claims 1, 8 and 17 from which claims 2-3, 11 and 21 depend, the AAPA fails to teach or disclose such a memory device that begins an iterating initialization cycle upon receiving a power signal, and stops the iterating initialization cycle upon receiving an external command. As such, the AAPA fails to teach or disclose independent claims 1, 8 and 17 and

therefore does not teach or suggest all elements of claims 2-3, 11 and 21. In addition, Applicant respectfully maintains that cited reference ST10F166 discloses a microcontroller with an internal 256k Flash memory and thus submits that ST10F166 also does not teach disclose such a memory device that begins an iterating initialization cycle upon receiving a power signal, and stops the iterating initialization cycle upon receiving an external command. Therefore combining the elements of the AAPA with cited reference ST10F166 does not teach or suggest all elements of claims 1, 8 and 17. The Applicant therefore maintains that claims 1, 8 and 17 are thus allowable over the AAPA and cited reference ST10F166, either alone or in combination. As claims 2-3, 11 and 21 depend from and further define claims 1, 8 and 17, claims 2-3, 11 and 21 are also deemed allowable.

In regards to independent claims 15 and 16, the Applicant respectfully submits that, as stated above, the AAPA fails to teach or disclose such a memory device that begins an iterating initialization cycle upon receiving a power signal, and stops the iterating initialization cycle upon receiving an external command. As such, the AAPA fails to teach or suggest all elements of claims 15 and 16. In addition, cited reference ST10F166 also does not teach disclose such a memory device that begins an iterating initialization cycle upon receiving a power signal, and stops the iterating initialization cycle upon receiving an external command. Therefore combining the elements of the AAPA with the cited reference ST10F166 does not teach or suggest all elements of claims 15 and 16. The Applicant therefore maintains that claims 15 and 16 are thus allowable over the AAPA and cited reference ST10F166., either alone or in combination.

Applicant respectfully contends that claims 2-3, 11, 21, and 15-16 as pending have been shown to be patentably distinct from the cited references, either alone or in combination. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 2-3, 11, 21, and 15-16.

Claim 32 was rejected under 35 U.S.C. § 103(a) as being anticipated by the Applicant's admitted prior art (the AAPA). Applicant respectfully traverses this rejection and feels that claim 32 is allowable for the following reasons.

Applicant respectfully notes that, as stated above in regards to the rejection of independent claim 28 from which claim 32 depends, the AAPA fails to teach or disclose such a memory device that begins an iterating initialization cycle upon receiving a power signal, and

stops the iterating initialization cycle upon receiving an external command. As such, the AAPA fails to teach or disclose independent claim 28 and therefore does not teach or suggest all elements of claim 32.

CONCLUSION

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

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